Application No.: 09/677,913 Docket No.: 21806-00106-US

REMARKS

Claims 1-15 are rejected. Favorable reconsideration of the application is requested.

Withdrawal of the rejection of claim 8 under 35 U.S.C. § 112 is requested. Claim 8 has been amended to more closely reflect the language of the specification. Specifically, page 6, lines 17-23 identify the fact that the degree of granularity utilized would depend on the accuracy of the model needed in order to achieve acceptable results as determined by user. This fully supports claim 8 as amended, and favorable reconsideration is believed to be in order.

Withdrawal of the rejection of claims 1-4, 7, 9 and 11-15 under 35 U.S.C. § 102(a) as being anticipated by Buffet et al. ("Methodology for I/O Cell Placement and Checking in ASIC Designs Using Area-Array Power Grid") is requested. The cited reference is directed to replacement of I/O cells in a basic design. An analysis technique is disclosed which models the power grid of an ASIC, and analyzes the ground buss, and the power supply buss. A simulation tool simulates the power grid, and analyzes the area between two ground and two VDD bumps contained within a window. A 3D resistance network having current sources representing currents to the I/O cells and logic cells surrounding the I/O cell is analyzed in the system. Rules are created for the IR drops from power bump to an I/O cell for each of the analysis windows. The simulation results establish a power grid structure supporting high current I/O cells meeting allowable IR and electromigration (EM) limits.

In reviewing the cited reference, there does not appear to be numerous elements identified in Applicants claims. In accordance with the present invention, a method for power distribution analysis for I/O currents in ASIC designs is described. According to, for instance, claim 1 a maximum and average current for each I/O circuit and an average logic current per node of an I/O circuit within a power distribution network are determined. In reviewing the reference, there does not appear to be any such average logic current demand utilized in the calculations.

Further, the present invention creates a resistance model of the power distribution network comprising nodes and resistors corresponding to points on busses of the network and resistivities corresponding to the points. While the cited reference does provide a model network, it's unclear that the model network represents nodes and resistors as set forth in the rejected claims. Indexing each of the I/O circuit currents and average logic current demand on a per node basis, then solving resistance and current source model voltages at each of the nodes is not disclosed in the cited reference. Thus, the present invention appears to describe a type of modeling which is not disclosed in the cited reference. The present invention does not rely upon as referenced, an analysis model which is a window comprising the area between two GND and two VDD bumps.

Claim 13, which is directed to a computer usable medium for carrying out the process in accordance with the invention, calls for solving for the voltage at nodes in terms of resistivities, I/O circuit currents and average logic current demand per node. It is submitted that the I/O circuit currents and average logic current demand are not shown or disclosed in the cited reference. Accordingly, each of the claims containing this limitation of the reference cannot yield or suggest the claimed subject matter.

Withdrawal of the rejection of the claims under 35 U.S.C. § 103 as being unpatentable over Buffet et al. is requested. Claim 5 is dependent on claim 1, and carries all the limitations thereof. Accordingly, claim 5 is considered to be allowable as well.

Withdrawal of the rejection of claims 6 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Buffet et al. in view of common knowledge regarding circuit analysis, is requested. Each of these claims depend on claim 1 and 7 respectively. The parent claims to these rejected claims all require that an average logic current demand per node be determined, additional to the currents of the I/O circuits, in performing the analysis. As the reference does not make any suggestion of these limitations, favorable reconsideration is believed to be in order.

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In view of the foregoing, an early allowance is solicited.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0456, under Order No. 21806-00106-US from which the undersigned is authorized to draw.

Dated: 7/29/04

Respectfully submitted,

By _____

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